

EXHIBIT A

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**TQ DELTA, LLC,
Plaintiff,**

V.

§§§§§

JURY TRIAL DEMANDED

COMMScope Holding Company, Inc., Commscope Inc., Arris International Limited, Arris Global Ltd., Arris US Holdings, Inc., Arris Solutions, Inc., Arris Technology, Inc., and Arris Enterprises, LLC,

Civil Action 2:21-cv-310-JRG
(Lead Case)

**NOKIA CORP., NOKIA SOLUTIONS
AND NETWORKS OY, and NOKIA OF
AMERICA CORP.**

§§§§§

Civil Action No. 2:21-cv-309-JRG
(Member Case)

Defendants.

**REBUTTAL EXPERT REPORT OF DR. TODOR COOKLEV
REGARDING VALIDITY OF THE FAMILY 2, 3, AND 9 PATENTS**

Dated: November 18, 2022

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Todor Cooklev, Ph.D.

receive and transmit data. Fadavi-Ardekani, at 7:25-30, explains that in the “optimal implementation,” using “full interleaver depth” of an ADSL session, “16 K of interleave & deinterleave” memory will be used. But in the same paragraph of Fadavi-Ardekani, he had just explained that full interleaver depth of an ADSL session requires 16 K for interleaving and 2 K for deinterleaving. *Id.* at 7:13-16. Thus, Fadavi-Ardekani’s “optimal implementation” proposes to use 2 K or the memory to perform both interleaving and deinterleaving. This is impossible and, thus, inoperable. Data received (deinterleave data) during one cycle will be overwritten by transmit data (interleave data) during a subsequent cycle. The G.993.1 standard requires that “[t]he interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255.” G.993.1 at § 8.4.1. A POSITA would recognize that a codeword, after interleaving, will necessarily span multiple (typically many) DMT frames and that all the DMT frames will not be received during one cycle. Consequently, the deinterleaving operation cannot be completed during that cycle. However, during the next cycle the received deinterleave data will be overwritten with interleave data that must be interleaved and transmitted. This means that received data will not be correctly deinterleaved. This is an additional reason why a POSITA would be not have combined the teachings of the G.993.1 and Fadavi-Ardekani.

402. Finally, a POSITA would recognize that modifying Fadavi-Ardekani to use the initialization messages described in G.993.1 would add to complexity without any benefit. Further, in view of that fact that the memory sizes in Fadavi-Ardekani are “derived by multiplying the maximum codeword length by the maximum interleaver depth,” processing and using the initialization messages of G.993.1 would bring no benefit to Fadavi-Ardekani.

403. Dr. Wesel asserts that the G.993.1 Standard “complements and benefits Fadavi-Ardekani by providing those configuration messages and in particular the idea of using a configuration message to communicate the capabilities available for interleaving and deinterleaving, such as maximum interleaver memory.” Wesel Family 3 Report at ¶ 512; *see also* Wesel Family 3 Report at ¶ 499. I disagree. Fadavi-Ardekani provides each interleaver and deinterleaver with the maximum amount of memory contemplated by the relevant ADSL2 and G.Lite standards “derived by multiplying the maximum codeword length by the maximum interleaver depth.” Fadavi-Ardekani at 7:9-11. Thus, Fadavi-Ardekani does not need “a configuration message to communicate the capabilities available for interleaving and deinterleaving,” as Dr. Wesel contends.

404. For these reasons, a POSITA would not be motivated to combine the teachings of Fadavi-Ardekani and the G.993.1 Standard.

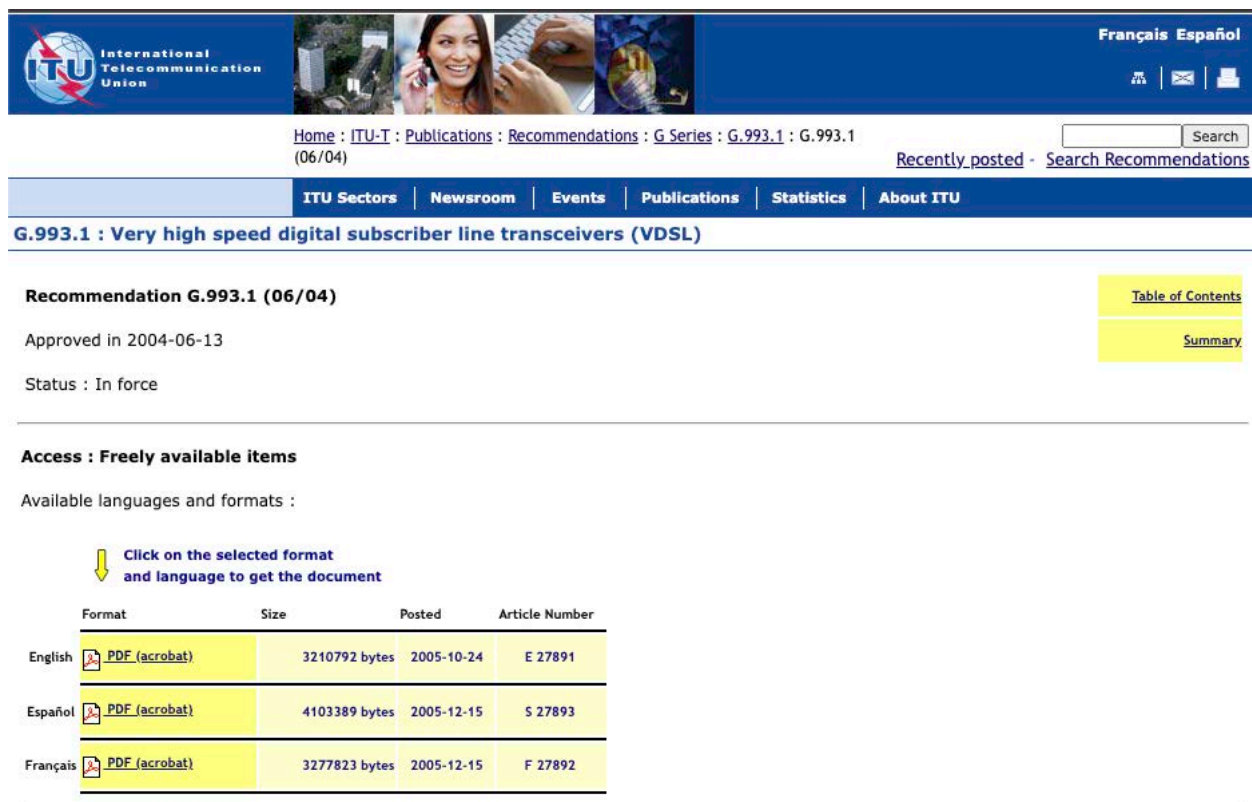
B. The Asserted Claims of the Family 3 Patents Are Not Obvious

1. The Family 3 Patents Are Valid Over the Combination of Mazzoni and G.993.1

405. Dr. Wesel has not shown that the claims of the Family 3 Patents would have been obvious. In addition to the reasons in the motivation to combine section above, the claims would have been obvious for at least the following reasons.

406. First, Dr. Wesel has not established that the version of the G.993.1 Standard he relies on was publicly available prior to the earliest priority date of the Asserted Patents. Specifically, for his invalidity opinions, Dr. Wesel relies on a version of the G.933.1 Standard (NOK00082901, COMMScope008135) that he suggests has an effective date of June 2004. This document is referred to herein as “the G.993.1 Standard.” But June 2004 date for the G.993.1

Standard is the date that a version of this standard was merely approved by an internal study group of the ITU-T (*see* G.993.1 Standard at p. i (ITU-T Recommendation G.993.1 was approved on 13 June 2004 by ITU-T Study Group 15 (2001-2004) under the ITU-T Recommendation A.8 procedure.”), not the date of its publication. The G.993.1 Standard Dr. Wesel relies on was not first published or first publicly available until October 24, 2005 per the ITU-T’s website, showing that the standard posted on October 24, 2005 (<https://www.itu.int/rec/T-REC-G.993.1-200406-I/en>).



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G.993.1 : Very high speed digital subscriber line transceivers (VDSL)

Recommendation G.993.1 (06/04)

Approved in 2004-06-13

Status : In force




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407. The Asserted Patents claim the benefit of the October 12, 2004 filing date accorded to the 269 provisional application. Additionally, the Asserted Patents claim priority to non-provisional application 11/246,163, filed on October 11, 2005. Because the G.993.1 Standard was not publicly available, i.e., published, until after the filing date of the provisional and non-provisional applications, the G.993.1 Standard is not prior art.

408. My opinion regarding the lack of public availability of the G.993.1 Standard until October 24, 2005 has been by Defendant CommScope. Specifically, as part its Family 6 *Markman* brief filed in the 2Wire case, CommScope stated that “[t]he June 2004 version of the G.993.1 Recommendation was merely *approved* in June of 2004. However, it was not *released to the public* until October 24, 2005[.]”. Defendants’ Answering Claim Construction Brief for the Family 6 Patents, *TQ Delta LLC v. 2Wire, Inc.*, No. 13-CV-1835-RGA (D. Del.), at p. 14. Thus, there is no genuine dispute that the G.993.1 Standard was not publicly accessible prior to the inventions claimed by the Asserted Patents. Accordingly, G.993.1 was not “published” until October 24, 2005 and does not qualify as prior art to the Asserted Claims.

409. Second, the combination would not disclose each of the claim elements for the asserted claims because the combination does not disclose a shared memory. There is no allegation that G.933.1 Standard contains a shared memory, and my opinion is that it does not.

410. Mazzoni does not disclose the shared memory claim elements. As detailed above, Mazzoni describes a predetermined assignment of a service that has a predetermined pair of upstream and downstream bit rates and a corresponding set of predetermined interleaver and deinterleaver parameter values (I, M, I’ and M’). Mazzoni at 3:62–4:14 (describing preset bit rates); *id.* at 6:11–53 (describing calculation of I, M, I’, and M’ for services based on bitrates). Mazzoni contemplates that a technician installing the modem would provide only a single one of the fixed services for a particular connection. *Id.* at 6:55–59 (“When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD may retrieve the corresponding values of I, M, I’ and M’ from the stored table.”). There is no disclosure that, once fixed at installation, any portion of the memory dedicated to the interleaver could ever be used by the deinterleaver and, conversely, that any portion of the memory dedicated

to the deinterleaver could ever be used by the interleaver. All that is disclosed are ways to divide the memory (MM) into two fixed memories. That is not shared memory, as construed.

411. Dr. Wesel generally focuses on the general disclosure of the MCD delivering the parameters as evidence that the memory allocation could be changed, namely the following two sentences (Mazzoni at 5:21–24).

As explained in more detail hereinafter, the parameters I, M, I' and M' can be modified, e.g., by software, and are delivered by control means MCD (see FIG. 3). The control means MCD may also be implemented in software.

412. These sentences, however, do not disclose a shared memory. They simply convey that the MCD may be implemented in software and “[a]s explained in more detail hereinafter,” how those parameters can be “modified.” *Id.* The only description “hereinafter” is that the “modification” is during installation of the modem by looking up a preset value in a table. *Id.* at 6:51–61.

413. There is no disclosure that a portion of the memory can be used by the interleaver at one point in time and the deinterleaver at another point in time. Indeed, CommScope’s prior expert testified that Mazzoni’s parameters were frozen upon installation (such as by a technician), there was no disclosure of changing the setting (or the process of sending out a technician), and the reference’s disclosure was “very limiting” in this regard. May 22, 2019 Trial Transcript in *TQ Delta LLC v. 2Wire, Inc.*, Civil Action No. 1:13-CV-01835-RGA (D. Del.) at 671:23–674:3.

414. Third, the combination would not disclose each of the claim elements for the asserted claims because the combination does not disclose the claimed message. There is no allegation that Mazzoni disclosed the claimed message, and my opinion is that it does not.

415. Nowhere in Mazzoni is there a message during initialization relating to the interleaver parameters. Nor is there any disclosure that Mazzoni allocates memory based on a

422. LB-031 also does not disclose the claimed message. As detailed above, LB-031 (like G.993.1) discloses that each side of the communication (the VTU-O and VTU-R) sends their maximum memory capabilities in each direction (using interleaver delay), and the system selects the smaller of the two. This message is not related to allocating memory; indeed, LB-031 describes that the allocation of upstream interleaver/deinterleaver memory occurs independently of the allocation of downstream interleaver/deinterleaver memory. LB-031 at 3. Accordingly, LB-031 teaches the use of dedicated memory and not a message related to allocating shared memory. In addition, as detailed above, combining Mazzoni with LB-031 would exceed the memory limits of Mazzoni.

3. The Family 3 Patents Are Valid Over the Combination of Fadavi-Ardekani and the G.993.1 Standard

423. Dr. Wesel has not shown that the claims of the Family 3 Patents would have been obvious. In addition to the reasons in the motivation to combine section above, the claims would have been obvious for at least the following reasons.

424. First, as I previously noted, Dr. Wesel has not established that the G.993.1 Standard was publicly available at the time of the inventions of the Asserted Patents. I have separately established that the G.993.1 Standard was in fact published after the priority date of the earliest filed non-provisional application and over a year after the filing date accorded to the provisional application. For this independent reason, the combination of Fadavi-Ardekani in combination with the G.993.1 Standard does not render the Asserted Claims obvious.

425. Second, the combination would not disclose each of the claim elements for the asserted claims because the combination does not disclose a shared memory. There is no allegation that G.933.1 Standard contains a shared memory, and my opinion is that it does not.